What is claimed is:

1. A camouflaged circuit structure having a gate region, including:

a substrate;

a first active region of a first conductivity type being disposed in said substrate;

a second active region of a first conductivity type being disposed in said substrate; and

a first well of said first conductivity type being disposed in said substrate under said gate region, said first well being in physical contact with said first active region and said second active region,

wherein said first well provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit.

2. The camouflaged circuit structure of claim 1 further comprising a plurality of wells of a second type, at least one of said plurality of wells of a second type being in physical contact with said first active region.

3. The camouflaged circuit structure of claim 2 wherein at least one of said plurality of wells is separated from said first well by a minimum first conductivity type to second conductivity type separation.

4. The camouflaged circuit structure of claim 2 wherein said first well is deeper than said plurality of wells of a second type.

5. The camouflaged circuit structure of claim 1 where said first well is deeper than said first and second active regions.

6. A semiconductor circuit comprising:

a substrate having a gate region;

a plurality of active regions of a first conductivity type disposed in said substrate, at least two of said plurality of active regions being separated from one another by said gate region;

a first well of said first conductivity type disposed in said substrate under said gate region and in physical contact with said at least two of said plurality of said active regions; and

a plurality of wells of a second type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second type are separated from said first well.

7. A method of camouflaging a circuit comprising the steps of:

fabricating a device having a gate region in a substrate of a first conductivity type, said device having at least two active regions of a second conductivity type; and

inserting a first well beneath said gate region, said first well beneath said gate region having a second conductivity type, said first well beneath said gate region being in physical contact with said at least two active regions, said first well beneath said gate region providing an electrical path between said at least two active regions regardless of a reasonable voltage applied to said gate region.

8. The method of claim 7 wherein said step of inserting a first well beneath said gate region includes the step of driving in said first well beneath said gate region such that said well beneath said gate region is deeper than said at least two active regions.

9. The method of claim 8, said method further comprising the step of inserting a second well having a first conductivity type beneath at least a portion of at least one of said at least two active regions, said second well being separated from said first well by a minimum first conductivity type to second conductivity type separation.

10. The method of claim 9 wherein said first well beneath said gate region is deeper than said second well.

11. A method of forming a CMOS circuit comprising the steps of:
modifying a conventional double well manufacturing process, wherein a conventional well of a first conductivity type is replaced with a well of a second conductivity type.

12. The method of claim 11 wherein said CMOS device comprises a plurality of active regions, said well of a second conductivity type being deeper than said active regions.

13. The method of claim 11 further comprising the step of forming at least one additional well of a first conductivity type, said well of a second conductivity type being shallower than said at least one additional well.